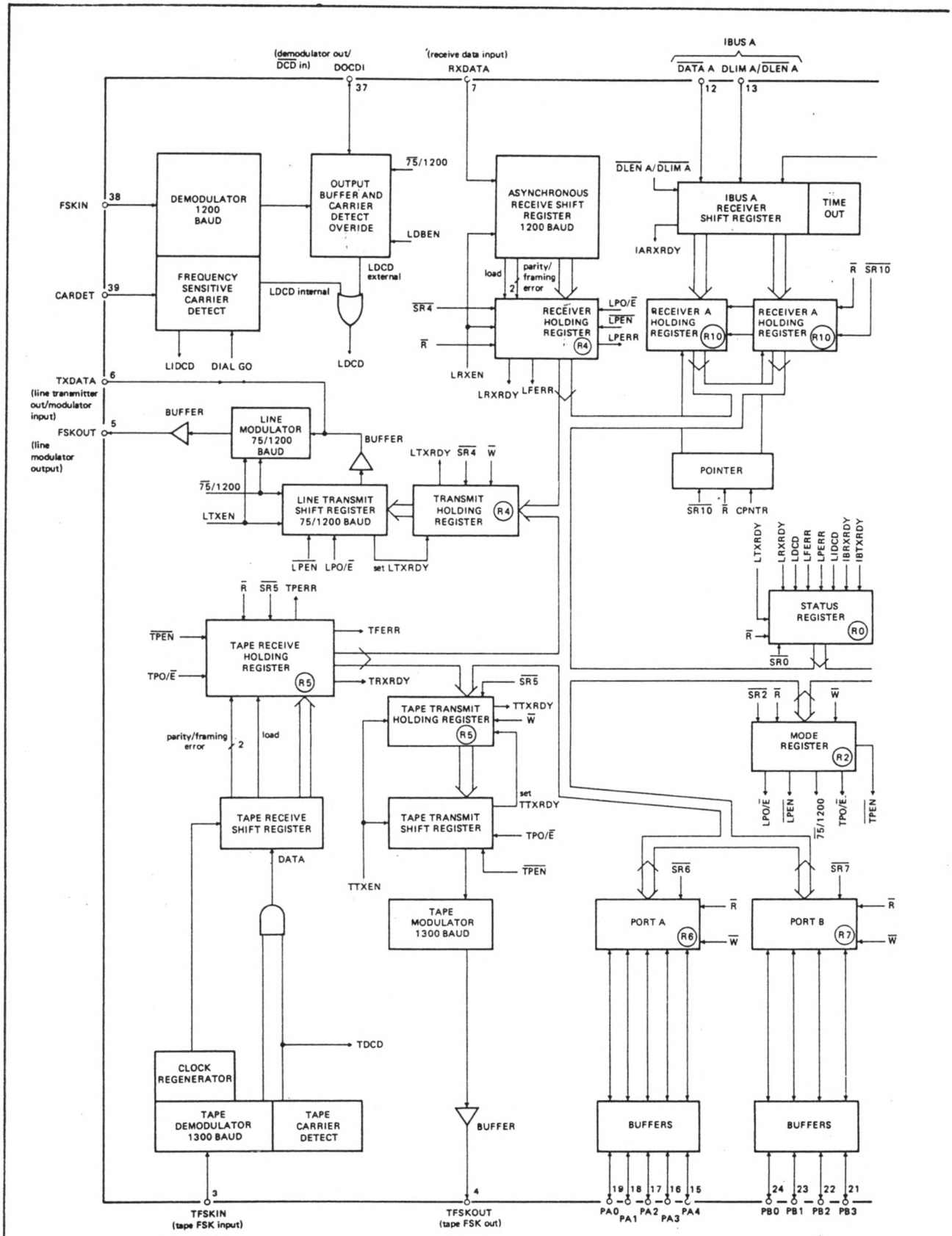
## APPENDIX 2

### Detailed description of organisation and features of SAA5070

#### INTERNAL ORGANISATION

A block diagram indicating the internal organisation of the SAA5070 is shown in Fig.60 and the pinning details are listed in Table 2. All the operating frequencies are supplied by a 1 MHz clock. Each section of the IC can communicate with a microprocessor via a register (of up to eight bits) which is connected to an internal bus. There are 15 registers on the IC, accessed by 11 addresses. Some of the registers are two-level, in which case two bytes are transferred by two successive read, or write, sequences to the same address, and in addition, some read-only registers have the same address as a write-only register. Table 3 lists the registers and their contents, while Table 4 lists the mnemonics used.

The majority of the registers are associated with a particular section of the IC. For example, the Dial Control and Timing Register is part of the autodial section. However, four of the registers – the Status Registers R0 and R1, the Mode Register R2, and the Command Register R3 – have functions which affect the whole IC. They indicate the current status of the device, determine the mode of operation, or initiate a specific function. The status registers are read-only, while the mode and command registers are read and write. Each section of the IC is now described in detail, the associated registers, flags, and pins being identified, and the method of operation explained.


(demodulator out/ DCD in)
DOCDI
37
(receive data input)
RXDATA
7
IBUS A
DATA A DLIM A/DLEN A
12
13
FSKIN
38
DEMODULATOR 1200 BAUD
OUTPUT BUFFER AND CARRIER DETECT OVERIDE
75/1200
LDBEN
LDCD external
ASYNCHRONOUS RECEIVE SHIFT REGISTER 1200 BAUD
DLEN A/DLIM A
IBUS A RECEIVER SHIFT REGISTER
TIME OUT
IARXRDY
CARDET
39
FREQUENCY SENSITIVE CARRIER DETECT
LDCD internal
load
parity/ framing error
2
R SR10
SR4
RECEIVER HOLDING REGISTER
R4
LPO/E
LPEN
LPERR
RECEIVER A HOLDING REGISTER
R10
RECEIVER A HOLDING REGISTER
R10
R
LIDCD
DIAL GO
LDCD
LRXEN
LRXRDY
LFERR
TXDATA
6
(line transmitter out/modulator input)
FSKOUT
5
(line modulator output)
BUFFER
LINE MODULATOR 75/1200 BAUD
BUFFER
LTXRDY SR4 W
POINTER
SR10 R CPNTR
75/1200
LTXEN
LINE TRANSMIT SHIFT REGISTER 75/1200 BAUD
TRANSMIT HOLDING REGISTER
R4
LPEN LPO/E
set LTXRDY
LTXRDY
LRXRDY
LDCD
LFERR
LPERR
LIDCD
IBRXRDY
IBTXRDY
STATUS REGISTER
R0
R
SR0
R SR5 TPERR
TPEN
TAPE RECEIVE HOLDING REGISTER
R5
TFERR
TPO/E
TRXRDY
SR5
TAPE TRANSMIT HOLDING REGISTER
R5
TTXRDY
W
SR2 R W
MODE REGISTER
R2
parity/framing error
2
load
TAPE RECEIVE SHIFT REGISTER
set TTXRDY
TAPE TRANSMIT SHIFT REGISTER
TPO/E
TPEN
LPO/E
LPEN
75/1200
TPO/E
TPEN
DATA
TTXEN
SR6
SR7
PORT A
R6
R
W
PORT B
R7
R
W
TAPE MODULATOR 1300 BAUD
TDCD
CLOCK REGENERATOR
TAPE DEMODULATOR 1300 BAUD
TAPE CARRIER DETECT
BUFFER
BUFFERS
BUFFERS
3
4
19 18 17 16 15
24 23 22 21
TFSKIN
(tape FSK input)
TFSKOUT
(tape FSK out)
PA0 PA1 PA2 PA3 PA4
PB0 PB1 PB2 PB3

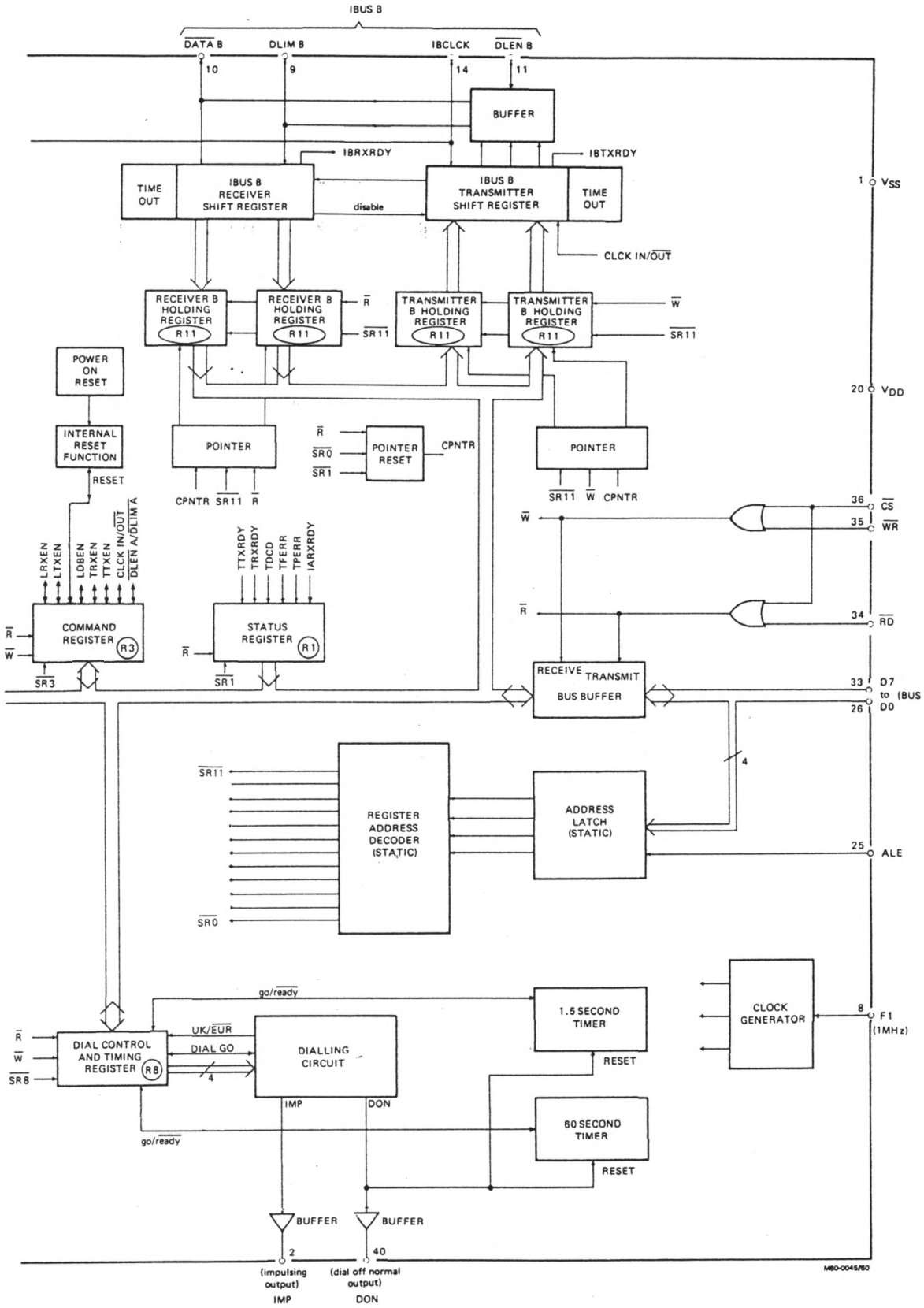



Fig.60 – Block diagram of SAA5070

**TABLE 2**

**Pinning details**

| Pin | Signal | Function |
|---|---|---|
| 1 | $V_{SS}$ | ground |
| 2 | IMP | output for dialling relay (impulsing) |
| 3 | TFSKIN | FSK input for tape section |
| 4 | TFSKOUT | output for FSK modulated data from tape section |
| 5 | FSKOUT | line modulator output |
| 6 | TXDATA | transmitter output; also modulator input if an external transmitter is used |
| 7 | RXDATA | data input for line receiver |
| 8 | F1 | input for 1 MHz clock |
| 9 | DLIM B | receiver B data clock input or transmitter B data clock output |
| 10 | $\overline{\text{DATA}}$ B | receiver B data input or transmitter B data output |
| 11 | $\overline{\text{DLEN}}$ B | receiver B bus-enable input or transmitter B bus-enable output |
| 12 | $\overline{\text{DATA}}$ A | receiver A data input |
| 13 | DLIM A/$\overline{\text{DLEN}}$ A | input for receiver A data clock or bus-enable signal |
| 14 | IBCLCK | input/output for 62.5 kHz clock |
| 15 to 19 | PA4 to PA0 | general-purpose input/output pins for Port A |
| 20 | $V_{DD}$ | 5 V supply |
| 21 to 24 | PB3 to PB0 | general-purpose input/output pins for Port B |
| 25 | ALE | input for address latch enable signal from microprocessor |
| 26 to 33 | D0 to D7 | input/output port for 8-bit microprocessor data bus |
| 34 | $\overline{\text{RD}}$ | input for read pulse from microprocessor |
| 35 | $\overline{\text{WR}}$ | input for write pulse from microprocessor |
| 36 | $\overline{\text{CS}}$ | chip-select input |
| 37 | DOCDI | demodulator output, input for external carrier detect |
| 38 | FSKIN | input for filtered and squared-up FSK signal |
| 39 | CARDET | input for unfiltered and squared-up FSK signal |
| 40 | DON | output for dialling relay (dial-off-normal) |

## TABLE 3

### SAA5070 register map

| Register | Address | Bit number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Status Register 0 | R0 | LTXRDY | LRXRDY | LDCD | LFERR | LPERR | LIDCD | IBRXRDY | IBTXRDY |
| | | R | R | R | R | R | R | R | R |
| Status Register 1 | R1 | TTXRDY | TRXRDY | TDCD | TFERR | TPERR | | IARXRDY | |
| | | R | R | R | R | R | | R | |
| Mode Register | R2 | LPO/$\overline{E}$ | $\overline{LPEN}$ | $\overline{75}$/1200 | | TPO/$\overline{E}$ | $\overline{TPEN}$ | | |
| | | R/W | R/W | R/W | | R/W | R/W | | |
| Command Register | R3 | LRXEN | LTXEN | RESET | LDBEN | TRXEN | TTXEN | CLCK IN/$\overline{OUT}$ | $\overline{DLEN}$ A/$\overline{DLIM}$ A |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Line Receiver Holding Register | R4 | Parity or B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | R | R | R | R | R | R | R | R |
| Line Transmit Holding Register | R4 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | W | W | W | W | W | W | W | W |
| Tape Receive Holding Register | R5 | Parity or B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | R | B | R | R | R | R | R | R |
| Tape Transmit Holding Register | R5 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | W | W | W | W | W | W | W | W |
| Port A | R6 | | | | PA4 | PA3 | PA2 | PA1 | PA0 |
| | | | | | R/W | R/W | R/W | R/W | R/W |
| Port B | R7 | | | | | PB3 | PB2 | PB1 | PB0 |
| | | | | | | R/W | R/W | R/W | R/W |
| Dial Control and Timing Register | R8 | UK/$\overline{EUR}$ | 60 s Timer | DIAL GO | 1.5 s Timer | DI3 | DI2 | DI1 | DI0 |
| | | R/W | R/W | R/W | R/W | W | W | W | W |
| IBUS A Registers (first byte) | R10 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | R | R | R | R | R | R | R | R |
| IBUS A Registers (second byte) | R10 | WL3 | WL2 | WL1 | WL0 | B12 | B11 | B10 | B9 |
| | | R | R | R | R | R | R | R | R |
| IBUS B Registers (first byte) | R11 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| IBUS B Registers (second byte) | R11 | WL3 | WL2 | WL1 | WL0 | B12 | B11 | B10 | B9 |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note R9 is unused

**TABLE 4 SAA5070 mnemonics**

| | |
|---|---|
| ALE | address latch enable signal from microprocessor |
| CLCK IN/$\overline{\text{OUT}}$ | input/output control for 62.5 kHz clock pin |
| CPNTR | pointer signal for two-byte registers |
| $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM A}}$ | three-wire/two-wire control for IBUS A receiver |
| DON | dial-off-normal (dialling relay) |
| IMP | impulsing (dialling relay) |
| IARXRDY | IBUS A receiver ready |
| IBRXRDY | IBUS B receiver ready |
| IBTXRDY | IBUS B transmitter ready |
| LDBEN | line demodulator output buffer enable |
| LDCD | line data carrier detected |
| LFERR | line receiver framing error |
| LIDCD | line instantaneous data carrier detect |
| $\overline{\text{LPEN}}$ | line parity enable |
| LPERR | line receiver parity error |
| LPO/$\overline{\text{E}}$ | line parity odd/even |
| LRXEN | line receiver enable |
| LRXRDY | line receiver ready |
| LTXEN | line tramsmitter and modulator enable |
| LTXRDY | line transmitter ready |
| TDCD | tape data carrier detected |
| TFERR | tape receiver framing error |
| $\overline{\text{TPEN}}$ | tape parity enable |
| TPERR | tape receiver parity error |
| TPO/$\overline{\text{E}}$ | tape parity odd/even |
| TRXEN | tape receiver enable |
| TRXRDY | tape receiver ready |
| TTXEN | tape transmitter enable |
| TTXRDY | tape transmitter ready |
| UK/$\overline{\text{EUR}}$ | impulsing ratio control for UK and European standards |
| $\overline{75}$/1200 | baud rate selection command for line modulator and line transmit shift register |
| $\overline{\text{SR0}}$ to $\overline{\text{SR11}}$ | internal register select signal |
| $\overline{\text{W}}$ | internal write signal |
| $\overline{\text{R}}$ | internal read signal |
| F1 | 1 MHz clock |

## Microprocessor interface

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| D0 to D7 | 26 to 33 | input/output port for 8-bit microprocessor data bus |
| ALE | 25 | input for address latch enable signal from microprocessor |
| $\overline{WR}$ | 35 | input for write pulse from microprocessor |
| $\overline{RD}$ | 34 | input for read pulse from microprocessor |
| $\overline{CS}$ | 36 | chip-select input |

*Operation*

The controlling microprocessor communicates with the SAA5070 via an 8-bit multiplexed address and data input/output port (pins 26 to 33). An internal read or write pulse ($\overline{R}$ or $\overline{W}$) is produced by gating $\overline{RD}$ or $\overline{WR}$ with $\overline{CS}$ (see Fig.60). A single register is enabled onto the internal bus of the IC by gating the read and write lines with the address decoder outputs $\overline{SR0}$ to $\overline{SR11}$. The register address is taken from the four least-significant data bits latched on the falling edge of the ALE signal (see timing diagrams Figs.61 and 62).

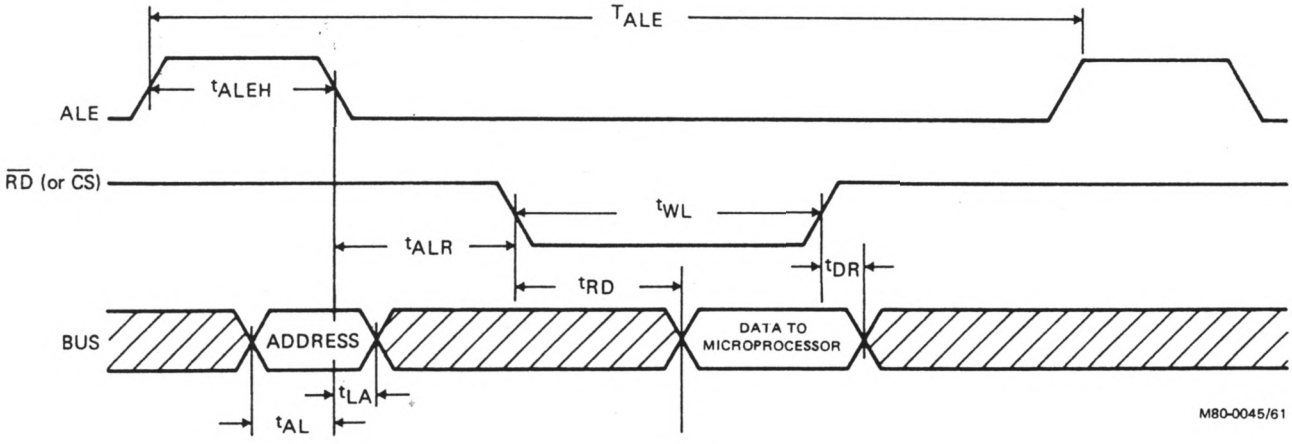



Fig.61 — Read cycle timing

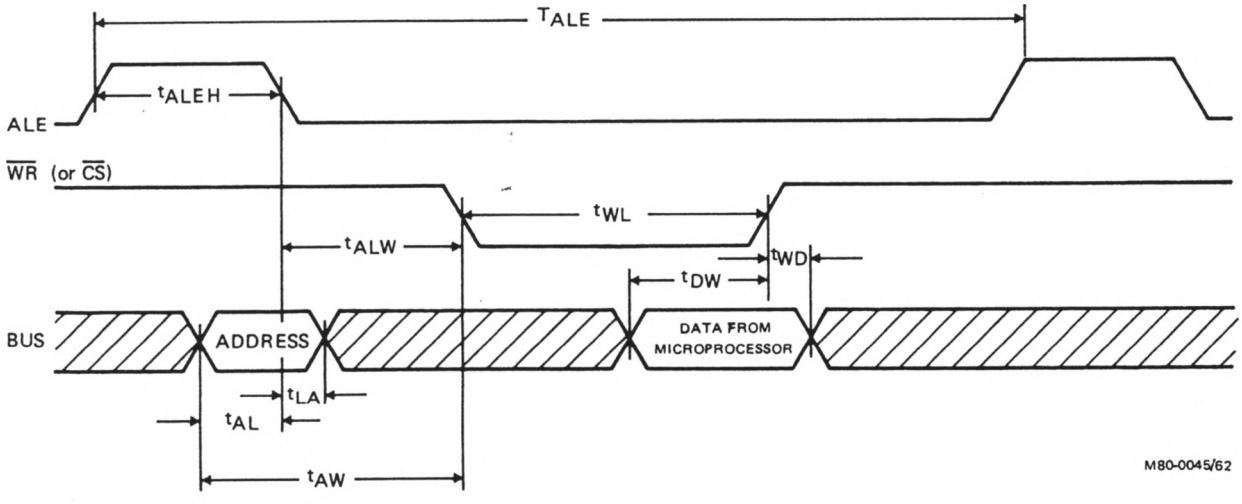



Fig.62 — Write cycle timing

## Autodial section

*Associated register*

R8 – Dial Control and Timing Register

| UK/$\overline{\text{EUR}}$ R/W 7 | 60s TIMER R/W 6 | DIAL GO R/W 5 | 1.5s TIMER R/W 4 | DI3 W 3 | DI2 W 2 | DI1 W 1 | DI0 W 0 |
|---|---|---|---|---|---|---|---|

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| DON | 40 | output for dialling relay (dial-off-normal) |
| IMP | 2 | output for dialling relay (impulsing) |

*Operation*

With bit 7 of R8 set to the desired state (see below), and the digit to be dialled held in bits 0 to 3, a dialling sequence is started by setting bit 5 (DIAL GO) HIGH. This initiates a sequence controller which loads the digit into a digit impulse counter. The counter then generates the required number of impulses, at the rate of 10 per second, together with the DON pulse which overlaps the impulses by about 7 ms (see Fig.63). The delay between successive digits, the inter-digit pause period, is generated by the sequence controller. Once a dialling sequence for one digit has been initiated, the register should be used only in the read mode. When the digit has been dialled the sequence controller resets bit 5 LOW, indicating to the microprocessor that the next digit to be dialled may be loaded into the register. Bit 5 is also used to inhibit the carrier detect circuit until dialling is complete (see below).

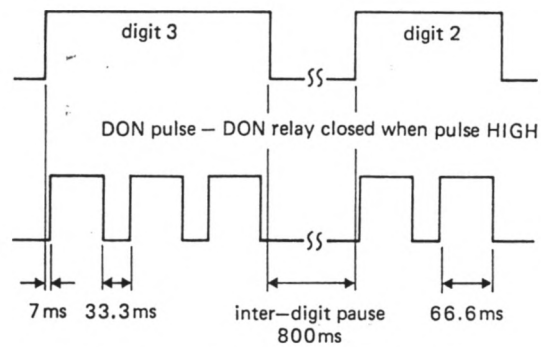



Fig.63 – Dialling pulse trains (UK standard)

Bit 7 (UK/$\overline{\text{EUR}}$) determines the mark/space ratio of the IMP pulses. This is 2:1 for the UK, and 1.5:1 for European requirements. In both cases the total pulse length is 100 ms.

There are timers associated with the dialling circuit which can be used to time out at 1.5 or 60 s by setting bits 4 or 6 HIGH respectively. The 60 s timer might typically be used to release the telephone line if connection has not been made within 60 s. The DON pulse resets the counter so that the time-out can be taken from the end of the last digit dialled.

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## Line demodulator and carrier detect

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| LIDCD | R0 (Status) | 2 | line instantaneous data carrier detect flag |
| LDCD | R0 (Status) | 5 | line data carrier detect flag |
| $\overline{75}$/1200 | R2 (Mode) | 5 | transmit baud rate selection |
| LDBEN | R3 (Command) | 4 | enables line demodulator output buffer |
| DIAL GO | R8 (Dial Control) | 5 | disables carrier detect circuit during dialling sequence |

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| FSKIN | 38 | input for filtered and squared-up FSK signal |
| CARDET | 39 | input for unfiltered and squared-up FSK signal |
| DOCDI | 37 | demodulator output or input for external carrier detect |

*Operation*

The demodulator circuit takes as its input the previously filtered and squared-up FSK signal from the telephone line. This signal is input via the FSKIN pin. The circuit outputs a pseudo-analogue varying mark/space ratio signal from the DOCDI pin which must be externally

filtered and squared-up to produce the digital data suitable for the RXDATA input.

Included with the demodulator is a carrier detect circuit which can operate in the following three ways.

1) Viewdata mode (1200 baud receive, 75 baud transmit). With LDBEN set HIGH, and DIAL GO and $\overline{75}$/1200 set LOW, the unfiltered squared-up FSK signal is input via the CARDET pin. The circuit identifies carrier by timing between successive zero crossings, the LIDCD flag being set HIGH when the signal falls within a narrow frequency window centred on 1.3 kHz. When LIDCD has been HIGH for a net time of 2 s, the LDCD flag is set HIGH to signify that carrier has been detected. This in turn enables the demodulator output pin (DOCDI) and widens the frequency window to include 2.1 kHz. At the same time, the CARDET input is disabled and the FSKIN input is enabled. If a valid signal is removed from the FSKIN pin for more than one second, then LDCD is reset LOW.
2) 1200 baud mode (1200 baud receive, 1200 baud transmit). Setting the $\overline{75}$/1200 flag HIGH disables the CARDET input and enables the FSKIN input. Only LIDCD is active in this mode, LDCD being forced LOW. LDBEN directly enables the output of the demodulator.
3) With an external modem. The carrier detect output of the external modem (active LOW) is now fed to the DOCDI pin of the demodulator. When the demodulator is disabled by the absence of a carrier, or LDBEN set LOW, the DOCDI output function goes HIGH allowing the external carrier detect signal to pull it LOW when required. This sets the LDCD flag HIGH.

## Line receiver

*Associated register*

R4 – Line Receive Holding Register, read-only

| PARITY or B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |
|---|---|---|---|---|---|---|---|
| R | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| LRXRDY | R0 (Status) | 6 | indicates data available in line receive holding register |
| LFERR | R0 (Status) | 4 | indicates framing error |
| LPERR | R0 (Status) | 3 | indicates parity error |
| LPO/$\overline{E}$ | R2 (Mode) | 7 | selects odd or even parity |
| $\overline{LPEN}$ | R2 (Mode) | 6 | enables or disables line parity detection |
| LRXEN | R3 (Command) | 7 | enables line receiver |

*Associated pin*

| Pin | Number | Function |
|---|---|---|
| RXDATA | 7 | data input for line receiver |

*Operation*

The receiver has a 52 times baud rate factor to cater for the maximum isochronous distortion. It may be configured to work with either seven data bits and a parity bit (flag $\overline{LPEN}$ set LOW), or with eight data bits and no parity check (flag $\overline{LPEN}$ set HIGH). Odd or even parity error detection may be selected via flag LPO/$\overline{E}$. Flag LPERR is set HIGH if a parity error is detected and flag LFERR is set HIGH if a framing error is detected. Before enabling the receiver, by setting the LRXEN flag HIGH, the required mode of operation should be selected via the $\overline{LPEN}$ and LPO/$\overline{E}$ flags.

The data format is ten bits per data word. This is made up of a start bit (LOW), eight data bits, the eighth being an optional parity bit, and a stop bit (HIGH). After the stop bit, the incoming data will remain HIGH until the next data word. When enabled, the receiver looks for a negative-going transition on the RXDATA input pin. After a half-bit period, the data is then sampled, and if LOW, this is interpreted as a start bit, initiating a sequence which clocks the data into a serial-to-parallel shift register. When the full 10-bit word has been received, the eight data bits are loaded into the line receive holding register (R4). The LRXRDY flag is then set HIGH, the complement of the stop bit is loaded into the LFERR latch, and the result of the parity check is loaded into the LPERR latch. If line parity is not enabled ($\overline{LPEN}$ set HIGH), then LPERR is held LOW. When R4 has been read, the LRXRDY flag is reset to LOW.

## Line transmitter

*Associated register*

R4 – Line Transmit Holding Register, write-only

| B8 W 7 | B7 W 6 | B6 W 5 | B5 W 4 | B4 W 3 | B3 W 2 | B2 W 1 | B1 W 0 |
|---|---|---|---|---|---|---|---|

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| LTXRDY | R0 (Status) | 7 | indicates when line transmit holding register is ready to accept new data |
| LPO/$\overline{E}$ | R2 (Mode) | 7 | selects odd or even parity |
| $\overline{LPEN}$ | R2 (Mode) | 6 | enables or disables parity |
| $\overline{75}$/1200 | R2 (Mode) | 5 | determines the transmission baud rate |
| LTXEN | R3 (Command) | 6 | enables the output of the line transmitter and the modulator |

*Associated pin*

| Pin | Number | Function |
|---|---|---|
| TXDATA | 6 | transmitter output, also modulator input if an external transmitter is used |

*Operation*

The data format of the transmitter is the same as that of the receiver, with parity controlled by the same flags. Two bit rates are available: 75 baud for viewdata transmissions, and 1200 baud for private communication systems. Selection is controlled via the $\overline{75}$/1200 flag. The transmitter and modulator may be used separately or together, and both are enabled by setting the LTXEN flag HIGH. When an external modem is used, the transmitter output is brought to the TXDATA pin. This pin is connected internally to the modulator input, and acts as the data input if the transmitter is off-chip. The TXDATA pin has an internal resistive pull-up permitting wire-AND connection. When an off-chip transmitter is used, data should not be written to the internal transmit holding register (R4), and a continuous HIGH signal is output from the TXDATA pin allowing control via the external 'UART'.

To operate the transmitter, the required mode should be established by writing the appropriate states of $\overline{75}$/1200, $\overline{LPEN}$, and LPO/$\overline{E}$ into the Mode Register (R2). The transmitter is enabled by setting the LTXEN flag HIGH in the Command Register (R3). The 8-bit data word is then written to the Transmit Holding Register (R4); this action sets the LTXRDY flag LOW. If the transmit shift register is not active, the contents of the holding register are transferred to the shift register, and the LTXRDY flag is reset HIGH so that new data may be written into the holding register. The start and stop bits together with the parity bit (if selected) are automatically written into the shift register together with the data word. The parity bit is calculated from the state of LPO/$\overline{E}$ and the 7-bit data word, the eighth bit being ignored.

---

## Line modulator

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| $\overline{75}$/1200 | R2 (Mode) | 5 | determines transmission baud rate |
| LTXEN | R3 (Command) | 6 | enables the output of the modulator and line transmitter |

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| TXDATA | 6 | transmitter output; also modulator input if an external transmitter is used |
| FSKOUT | 5 | line modulator output |

*Operation*

The modulator outputs a pseudo-analogue signal, which after minimal lowpass filtering provides a suitable FSK signal for the telephone line. One sinewave cycle consists of a 92-bit pattern, stored in an internal ROM (see Fig.64). The frequency coding of the FSK signal is dependent upon the transmission bit rate. At 1200 baud, a HIGH is represented by 1.3 kHz and a LOW by 2.1 kHz, while at 75 baud, HIGH and LOW signals are represented by 390 and 450 Hz respectively.

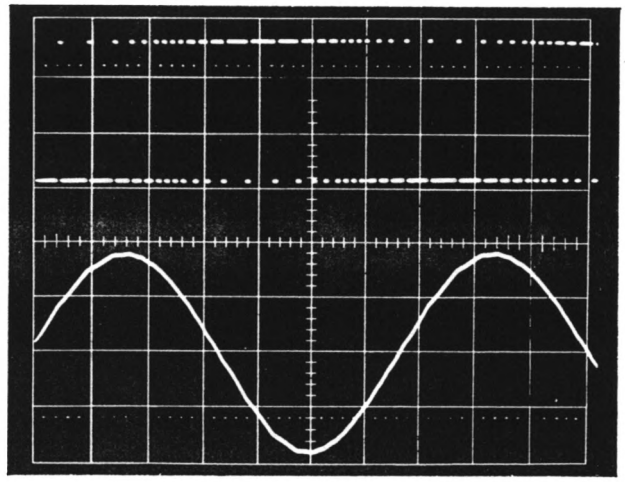

Fig.64 — Delta-modulated 390 Hz return channel signal:
upper trace — serial bit stream
lower trace — serial bit stream after lowpass filtering

## Tape section

*Associated registers*

R5 — Tape Receive Holding Register, read-only

| PARITY or B8 R 7 | B7 R 6 | B6 R 5 | B5 R 4 | B4 R 3 | B3 R 2 | B2 R 1 | B1 R 0 |
|---|---|---|---|---|---|---|---|

R5 — Tape Transmit Holding Register, write-only

| B8 W 7 | B7 W 6 | B6 W 5 | B5 W 4 | B4 W 3 | B3 W 2 | B2 W 1 | B1 W 0 |
|---|---|---|---|---|---|---|---|

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| TTXRDY | R1 (Status) | 7 | indicates when tape transmit holding register is ready to accept new data |
| TRXRDY | R1 (Status) | 6 | indicates when valid data is available in the tape receive holding register |
| TDCD | R1 (Status) | 5 | indicates detection of tape data carrier |
| TFERR | R1 (Status) | 4 | indicates framing error |
| TPERR | R1 (Status) | 3 | indicates parity error |
| TPO/$\overline{E}$ | R2 (Mode) | 3 | selects odd or even parity |
| $\overline{TPEN}$ | R2 (Mode) | 2 | enables or disables tape parity detection |
| TRXEN | R3 (Command) | 3 | enables tape receiver |
| TTXEN | R3 (Command) | 2 | enables tape transmitter |

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| TFSKIN | 3 | FSK input to tape section |
| TFSKOUT | 4 | output for FSK modulated data from tape section |

*Operation*

The tape data modulation system is a modified form of the 'Kansas City' standard. A HIGH is represented by one cycle of 1.3 kHz, and a LOW by two cycles of 2.6 kHz. The bit rate is 1300 baud, and the data format is identical to that for viewdata. The modulator output

requires only minimal external lowpass filtering to produce data suitable for audio cassette tape recorders. The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred directly (via the microprocessor) onto tape independently of possible tolerances in the line receive rate.

To overcome the tendency of cassette recorders to attenuate higher frequencies, the 1.3 kHz signal contains 2 $\mu$s-wide attenuating pulses every 12 $\mu$s. After external filtering, this reduces the 1.3 kHz signal by 3 dB relative to the 2.6 kHz signal.

To operate the tape section, the required parity mode should first be established by setting the required states of $\overline{\text{TPEN}}$ and TPO/$\overline{\text{E}}$ in the mode register (R2). Data is input and output via holding and shift registers (see Fig.60). The procedure for data transmission is described first.

The TTXEN flag enables the contents of the transmit shift register into the modulator, and should be set HIGH before data is written to the transmit holding register. With TTXEN set LOW, the modulator outputs a continuous 1.3 kHz signal. When a data word is written into the transmit holding register, the TTXRDY flag goes LOW. If the transmit shift register is not currently active, the contents of the holding register, together with a valid parity bit (if enabled) and the start and stop bits, are then transferred to the transmit shift register. The TTXRDY flag now goes HIGH, indicating that the transmit holding register is ready to accept a new data word. Output from the modulator is via the TFSKOUT pin.

Data from the tape recorder is input via the TFSKIN pin. Because the modulation is in phase with the data, a clock may be extracted from the signal on replay, and this permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag HIGH if a tape carrier signal (1.3 or 2.6 kHz) is received for 100 ms. If the carrier is lost for 100 ms, then the TDCD flag is reset LOW. The TDCD flag may be used by the microprocessor to determine when to enable the tape receiver by setting the TRXEN flag HIGH. With TRXEN set HIGH, data can be clocked into the receive shift register using the extracted clock. After ten clock periods, the eight data bits are loaded into the Tape Receive Holding Register, and the TRXRDY flag is set HIGH. The treatment of the stop and parity bits is identical to that described in the line receiver section (see above). The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register, and is reset LOW when the register has been read.

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## IBUS A receiver and IBUS B receiver/transmitter

*Associated registers*

R10 – Receiver A Holding Register (two-byte), read-only
R11 – Receiver B Holding Register (two-byte), read-only
R11 – Transmitter B Holding Register (two-byte), write-only

Each of the three two-byte registers has the same structure:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| first byte | B8 7 | B7 6 | B6 5 | B5 4 | B4 3 | B3 2 | B2 1 | B1 0 |
| second byte | WL3 7 | WL2 6 | WL1 5 | WL0 4 | B12 3 | B11 2 | B10 1 | B9 0 |

*Associated flags in other registers*

| Flag | Register | Bit | Function |
|---|---|---|---|
| IBRXRDY | R0 (Status) | 1 | indicates presence of valid data in receiver B holding register |
| IBTXRDY | R0 (Status) | 0 | indicates that transmitter B holding register is ready to accept new data |
| IARXRDY | R1 (Status) | 1 | indicates presence of valid data in receiver A holding register |
| CLCK IN/$\overline{\text{OUT}}$ | R3 (Command) | 1 | input/output control for IBCLCK pin (62.5 kHz) |
| $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM A}}$ | R3 (Command) | 0 | three-wire/two-wire control for IBUS A receiver |

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| $\overline{\text{DATA}}$ A | 12 | receiver A data input |
| DLIM A/$\overline{\text{DLEN}}$ A | 13 | input for receiver A data clock or bus-enable signal |
| $\overline{\text{DATA}}$ B | 10 | receiver B data input or transmitter B data output |
| DLIM B | 9 | receiver B data clock input or transmitter B data clock output |
| $\overline{\text{DLEN}}$ B | 11 | receiver B bus-enable input or transmitter B bus-enable output |
| IBCLCK | 14 | input/output for 62.5 kHz clock |

*Operation*

All three IBUS circuits, receiver A, receiver B, and transmitter B, are capable of handling variable length codes of 1 to 12 bits. In practice up to 15 bits may be transmitted, 12 being data and the remainder trailing zeros, and 15 bits can be received but only the last 12 will be retained. Each of the three circuits has two 8-bit registers, which are accessed by two successive read or write operations to the same address. A pointer circuit selects the appropriate byte via the signal CPNTR (see Fig.60). The pointer circuits are reset to select the first byte with power on, when bit 5 (RESET) is set in R3, or whenever the status registers R0 or R1 are read.

The structure of each of the three registers is indicated above. The first byte consists solely of data bits, while for the second byte, bits 0 to 3 are data bits and bits 4 to 7 specify the word length of the message. The bits are held strictly in the order in which they are received or transmitted, so that in the receivers B12 is always the last data bit received, while in the transmitter, B1 is always the first bit to be transmitted. This applies irrespective of the word length. For the transmitter, the word length is used to generate the correct number of data clock pulses, while for the receivers it may be used to identify the source of the message or to establish that the message is of valid length.

The IARXRDY and IBRXRDY flags are set HIGH when a message has been received by the IBUS A and IBUS B shift registers. With these flags set HIGH, the corresponding receiver holding registers cannot be overwritten until their contents have been read. Reading a holding register resets the corresponding IARXRDY or IBRXRDY flag. Transmitter B is initiated by writing two bytes to the Transmitter B Holding Register R11, which in turn sets the IBTXRDY flag LOW. The DLIM B line is then sampled until the line-free state is detected, when a time-out begins. If DLIM signals are detected before the end of the time-out period, then the time-out is reset and the search for the line-free state repeated. When the time-out is complete, the contents of the holding register are transferred to the shift register and word length counter. The data and the correct number of data clock pulses are then transmitted, after which the IBTXRDY flag is reset HIGH. Receiver B is inhibited from receiving the data transmitted from transmitter B.

Receiver A may operate either as a two-wire receiver with $\overline{\text{DATA}}$ and DLIM, or as a three-wire receiver with $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and IBCLCK. The desired option is selected via the $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM A}}$ flag. Setting this flag LOW gives two-wire operation; setting it HIGH gives three-wire operation. The DLIM signal for the IBUS A receiver is generated internally from the 62.5 kHz clock on the IBCLCK pin when in the three-wire mode. In addition to providing an input for the IBUS A receiver, the 62.5 kHz clock may be used to synchronise transmitter B outputs or to provide an output synchronous with transmitter B. The 62.5 kHz waveform may be either output from the IBCLCK pin or input from an external source. This function is selected by the CLCK IN/$\overline{\text{OUT}}$ flag in the command register (R3). The IBUS waveforms are shown in Fig.65.

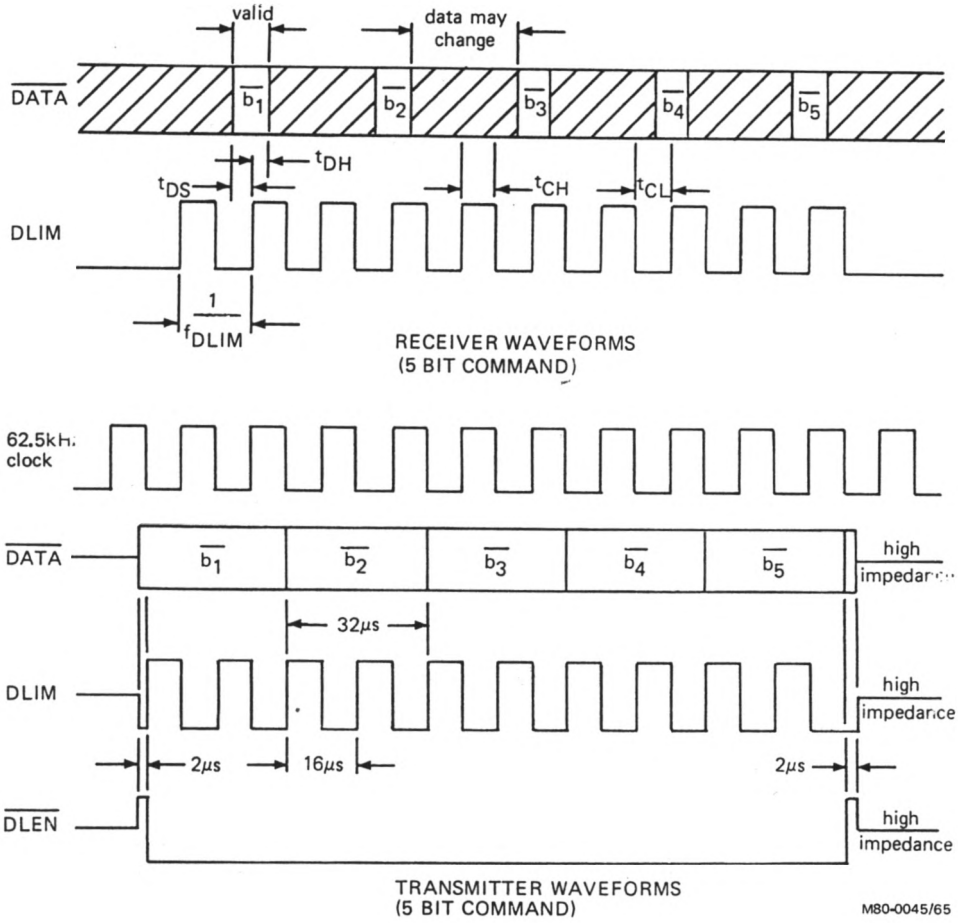


Fig.65 – IBUS waveforms

## Port A

*Associated register*
R6 – Port A, read/write

| | | | | |
|---|---|---|---|---|
| PA4 R/W 4 | PA3 R/W 3 | PA2 R/W 2 | PA1 R/W 1 | PA0 R/W 0 |

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| PA4 to PA0 | 15 to 19 | general-purpose input/output pins for Port A |

*Operation*
This is a 5-bit general-purpose input/output port. The outputs are latched and are open-drain up to a nominal 12 V. Any pin of the port may be used as an input if a HIGH is written to the corresponding output latch. This allows the external circuit to pull the pin LOW. The controlling microprocessor can determine the state of the pins by a read sequence to R6. If the supply to the open-drain outputs is turned on before the IC power supply, then before operation the port must first be cleared by writing a HIGH to each of the output latches.

Port A might typically be used in viewdata mode as an interface to an Electrically Alterable ROM (EAROM) in which can be stored telephone numbers and the user identification code.

## Port B

*Associated register*
R7 – Port B, read/write

| PB3 R/W 3 | PB2 R/W 2 | PB1 R/W 1 | PB0 R/W 0 |
|---|---|---|---|

*Associated pins*

| Pin | Number | Function |
|---|---|---|
| PB3 to PB0 | 21 to 24 | general-purpose input/output pins for Port B |

*Operation*
This is a 4-bit general-purpose input/output port. Its operation is essentially identical to Port A, except that access is now achieved by addressing R7, and outputs PB1 to PB3 are open-drain to a nominal 5 V. Output PB0 is open-drain to a nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture-On function.

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## Reset function

The SAA5070 may be set to its nominal state automatically at power-on via an internal power-on reset circuit or by setting bit 5 (RESET) in the Command Register (R3) HIGH. The RESET flag goes LOW at the end of the reset sequence. After reset, all the flags except three will be LOW giving normal viewdata operation. The three HIGH flags LTXRDY, IBTXRDY, and TTXRDY, indicate that the three IC transmitters are ready to accept data.

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